REMARKS

Double Patenting Rejection

Claims 11-14, 16, 17, 19 and 20 were provisionally rejected under the judicially created obviousness-type double patenting as being unpatentable over claims 11-20 of copending U.S. Patent Application Serial No. 11/436,803.

Due to the fact that neither the present application nor the '803 application have allowed claims, Applicant respectfully requests that the double patenting rejection be held in abeyance until all pending claims have been allowed. Upon allowance of the claims, Applicant will submit a terminal disclaimer to overcome the non-statutory double patenting rejection.

In the Claims

Claims 1-3, 5-13, 16-17 and 19-20 have been amended to more precisely define the Applicant's claimed subject matter. Applicant respectfully submits that the amendments are supported by the Specification as filed and thus do not constitute new matter. *See*, Specification, paragraph [0029]. ("For example, if the operating system receives a request to write data to logical memory address 10002H, it checks the table to determine that logical memory address maps to physical memory address 30002H.")

Claim Rejections Under 35 U.S.C. § 102

Claims 1-3 and 5-10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Borkenhagen et al. (U.S. Patent No. 5,067,105). Applicant respectfully traverses the rejection.

Applicant respectfully submits that Borkenhagen et al. does receive a logical address from a CPU. However, Borkenhagen et al. strips off the 6 most significant bits of the logical address provided by the CPU and performs a conversion operation on the 6 bits to yield a 3 bit logical card address. Borkenhagen et al., column 3, lines 59-64. The 3 bit logical card address is converted further by the physical card selector logic utilizing the card identification register to yield a 3 bit physical card address. Borkenhagen et al., Figure 1. The Applicant respectfully disagrees with the Examiner equating the card identification register of Borkenhagen et al. with the look-up table recited in claim 1. Office Action, page 4, section 2. Claim 1 recites, in part, the "look-up table having logical memory addresses with their corresponding physical memory

addresses." Applicant respectfully submits that the physical card address of Borkenhagen et al. and a physical memory address taken in the context of the present Specification and claim 1 are not equivalent. Claim 1 does not recite the look-up table comprising memory device (e.g. card) address information as does the card identification register of Borkenhagen et al. The look-up table recited in claim 1 maintains the actual logical memory addresses along with their associated physical memory addresses. This is distinguishable from the card identification register of Borkenhagen et al. which only maintains a card address that allows for the selection of a memory device (e.g. card) but does not provide the actual physical memory address location.

Applicant respectfully submits further that even if the card identification register of Borkenhagen et al. equated to the look-up table recited in claim 1, which Applicant contends it does not, the 3 bit logical card address does not comprise even a part of the received logical address. Borkenhagen et al. discloses that the 3 bit logical card address is generated by distilling down the 6 most significant bits of the logical address. Claim 1 recites a "look-up table having logical memory addresses with their corresponding physical memory addresses." If the received logical memory address is transformed, resulting in a 3 bit logical card address as in Borkenhagen et al., then accessing the look-up table of logical memory addresses as recited in claim 1 would serve no purpose as there would be no corresponding physical address for the 3 bit logical card address.

Applicant respectfully submits further that Borkenhagen et al. discloses that "the physical address is obtained from the logical address by a translation according to the invention." Borkenhagen et al., column 3, lines 21-23. Applicant submits that the "translation according to the invention" of Borkenhagen et al. comprises the striping off of the first 6 bits of the logical address provided by the CPU, a reduction of those 6 bits down to a 3 bit logical card address, a further translation of the 3 bit logical card address to a 3 bit physical card address wherein the physical address is generated by combining the physical card address with "a second portion of said logical memory address to obtain therefrom a physical memory address." *See*, Borkenhagen et al., Figure 1. *See also*, Borkenhagen et al., claim 1, part f. Applicant respectfully contends that this translation which is regarded as the invention of Borkenhagen et al. is distinctly different from "receiving a command comprising a first logical memory address from the range of logical memory addresses; accessing a look-up table having logical memory addresses with their corresponding physical memory addresses from one of the plurality of ranges of physical

memory addresses to find a first physical memory address, from a range of physical memory addresses, that corresponds to the first logical memory address" as recited in claim 1. There is no requirement recited in claim 1 for a method of translation such as in Borkenhagen et al. since the look up table is stored in memory and only a read operation is required to obtain the physical memory address corresponding to a received logical memory address. The method of Borkenhagen et al. involves deconstruction and modification of a part of the original logical address then a recombination with another part of the original logical address to obtain the final physical address. Thus, the present claims are to a completely different structure than that disclosed in Borkenhagen et al.

Applicant further respectfully submits that Borkenhagen et al. also fails to disclose "generating a chip select signal in response to the first physical memory address" as recited in claim 1. The Examiner asserts in the Office Action that generating a chip select signal is disclosed in Borkenhagen et al. as a result of "selecting a physical card based on the physical card address." Office Action, page 4, section 2. Applicant respectfully submits that the "chip select signal" of claim 1 is generated "in response to the first physical memory address." Borkenhagen et al. discloses that the physical memory address is formed by "combining said physical card address with a second portion of said logical memory address to obtain therefrom a physical memory address." Borkenhagen et al., claim 1, part f. Thus, Borkenhagen et al. discloses that the physical card address is only a part of the final physical address as defined by Borkenhagen et al. Claim 1 recites, in part, that the select signal is generated in response to the physical memory address. Thus, the physical card address of Borkenhagen et al. cannot be both a part of the physical address and also be a select signal that is generated in response to the physical address when the physical address of Borkenhagen et al. doesn't exist until the physical card address and the second portion of the logical address have been combined.

Applicant respectfully submits that for the reasons presented above that Borkenhagen et al. fails to disclose each and every element of claim 1 and that claim 1 is therefore in condition for allowance. Applicant also respectfully submits that due to the similarity of elements between claims 1 and 7 that claim 7 is also in condition for allowance for the same reasons as claim 1 discussed above. Applicant respectfully asserts further that claims 2-3, 5-6 and 8-10 are also in condition for allowance in that these claims depend from and further define their respective patentably distinct base claims 1 and 7.

Applicant therefore respectfully requests that the rejection of claim 1-3 and 5-10 under 35 U.S.C. § 102(b) as being anticipated by Borkenhagen et al. be reconsidered and withdrawn.

Claim Rejections Under 35 U.S.C. § 103

Claims 4, 11-14, 16, 17, 19 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Borkenhagen et al. (U.S. Patent No. 5,067,105) in view of Daberko (U.S. Patent No.5,787,445).

Applicant respectfully submits that claims 11, 13, 17 and 20, due to their similarity of elements with claim 1, are in condition for allowance for the same reasons as presented above with respect to claim 1.

Applicant respectfully submits further that Daberko merely discloses an "objective of making a system see flash memory as RAM." Daberko, column 3, lines 14-16. Applicant therefore respectfully submits that Daberko fails to overcome the deficiencies of Borkenhagen et al. with respect to claims 1, 11, 13, 17 and 20 and therefore asserts that these claims are in condition for allowance. Applicant therefore contends that claims 4, 12-14, 16 and 19 are also in condition for allowance in that these claims depend from and further define their respective patentably distinct base claims 1, 11, 13, 17 and 20.

Applicant therefore respectfully requests that the rejection of claims 4, 11-14, 16, 17, 19 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Borkenhagen et al. in view of Daberko be reconsidered and withdrawn.

CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. Please charge any further fees deemed necessary or credit any overpayment to Deposit Account No. 501373.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211.

Respectfully submitted,

Date: 11/02/07

Kenneth W. Bolvin
Reg. No. 34,125

Attorneys for Applicant
Leffert Jay & Polglaze
P.O. Box 581009
Minneapolis, MN 55458-1009
T (612) 312-2200
F (612) 312-2250